

FAST - [resistor.wap.1]

File View Edit Table Window Help

Active

- L1: (2879) (deep near trench\$1) or (bottle near trench\$1)
- L2: (4644) (deep near trench\$1) or (bottle near trench\$1) or (trench near
- L3: (433) 2 and (buried adj plate)
- L4: (215) 3 and (anneal\$3 or heat\$3)
- L5: (196) 4 and ((upper or top) with (trench or capacitor))
- L6: (118) 5 and (shap\$3 or configuration or rectangle or rectangular)
- L7: (103) 6 and trench.clm.
- L8: (93) 7 and (capacitor.clm. or memory.clm. or (buried adj plate).clm.)
- L9: (93) 8 and (etch\$3)
- L10: (29) 9 and ((ammonia or KOH or plasma) with etch\$3)
- L11: (433) 2 and (buried adj plate)
- L12: (349) 11 and (anneal\$3 or heat\$3 or thermal)
- L13: (235) 12 and ((etch\$3 or shap\$3 or remov\$3) near (trench or upper or
- L14: (0) 13 and ((upper or top) near (rectangle or rectangular))
- L15: (220) 13 and trench.clm.
- L16: (26) 15 and (rectangular or rectangle)
- L17: (9) ("5804851") or ("6004844") or ("6218319") or ("6281068") or ("6
- L18: (2547) 2 and trench.clm.
- L19: (32) 18 and ((wide\$3 or shap\$3 or etch\$3) near (upper or top) near t
- L20: (23) 18 and ((wide\$3 or shap\$3 or etch\$3) near (upper or top) adj t

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18 and ((wide\$3 or shap\$3 or etch\$3) near ((upper or top) adj trench))

	V	T	PT	P	Document ID	Issue Dat	Pages	Title	Current OP	Current XR	Retrieval	Inventor	S	C	3	4	5
13					US 6660582	20031209	28	Method of forming a vertical field-effect t	438/245	257/E21.65		Birner, Albert et al.					
14					US 6620699	20030916	8	Method for forming inside nitride spacer f	438/386	257/E21.65		Schoiz, Arnd et al.					
15					US 6503798	20030107	9	Low resistance strap for high density trench	438/268	257/301;		Divakaruni,					
16					US 6403412	20020611	10	Method for in-situ formation of bottle sha	438/238	257/E21.21		Ramachandra et al.					
17					US 6318384	20011120	37	Self cleaning method of forming deep trenches i	134/22.1	134/1.1;		Economikos,					
18					US 6180975	20010130	13	Depletion strap semiconductor memory de	257/306	257/296;		Laertis et al.					
19					US 5989975	19991123	8	Method for manufacturing shallow t	438/424	257/E21.54		Khan, Anisul et al.					
20					US 5395786	19950307	7	Method of making a DRAM cell with trench capaci	438/248	257/E21.65		Radens, Carl J. et al.					
21					US 5298790	19940329	7	Reactive ion etching buffer mask	257/622	257/301;		Hsu, Louis L. et al.					
22					US 5118384	19920602	5	Reactive ion etching buffer mask	438/717	257/534;		Harmon, David L. et al.					
23					US 4980747	19901225	8	Deep trench isolation with surface contact to	257/513	204/192.37		Harmon, David L. et al.					
									257/520;	257/E21.53		Hutter, Louis N. et al.					

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- ✎ L2: (1618) 1 and (deep or bottle)
- ✎ L3: (1134) 2 and ((buried adj plate\$1) or (deep near trench\$2))
- ✎ L4: (611) 3 and ((upper or lower or top or bottom) near (trench\$2 or capacitor\$2))
- ✎ L5: (599) 4 and etch\$3
- ✎ L6: (386) 5 and (ammonia or plasma or KOH or NH\$2 or hydroxide)
- ✎ L7: (337) 6 and trench\$2.clm.
- ✎ L8: (246) 7 and ((upper or top) near (trench or capacitor))
- ✎ L9: (136) 8 and (shap\$3 or configuration)
- ✎ L10: (84) 8 and ((upper or top) near trench\$2).clm.
- ✎ L11: (47) 10 and (shap\$3 or configuration)
- ✎ L12: (7) 11 and rectangular
- ✎ L13: (142) 7 and (etch\$3 near (ammonia or NH\$1 or KOH or potas\$2))
- ✎ L14: (85) 13 and (etch\$3 near (trench or capacitor))
- ✎ L15: (83) 14 and (etch\$3 near trench\$2)
- ✎ L16: (12) 15 and (etch\$3 near (upper or top))
- ✎ L17: (88) 3 and (buried adj plate).clm.
- ✎ L18: (34) 17 and dopant and anneal\$3
- ✎ L19: (15) 18 and (shap\$3 or configuration)
- ✎ L20: (15) 3 and (trench\$3 near (rectangular or rectangular))

[illegible]

	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OP	Current RA	Retrieval	Inventor	S	C	S	...	S
2	P	P	P	P	US 20030170951	20030911		Novel method to achieve increased trench depth.	438/243	257/E21.54		Chan, Kevin K. et al.	P	P	P	P	P
3	P	P	P	P	US 20010016398	20010823	17	METHOD FOR EXPANDING TRENCHES BY AN ISOTROPIC	438/427	257/E21.22		KUDELKA, STEPHAN et al.	P	P	P	P	P
4	P	P	P	P	US 6740555	20040525	11	Semiconductor structures and manufact	438/242	257/68;		Tews, Helmut Horst et al.	P	P	P	P	P
5	P	P	P	P	US 6605860	20030812	11	Semiconductor structures and manufact	257/618	257/619;		Tews, Helmut Horst et al.	P	P	P	P	P
6	P	P	P	P	US 6426254	20020730	16	Method for expanding trenches by an isotropic	438/245	257/E21.22		Kudelka, Stephen et al.	P	P	P	P	P
7	P	P	P	P	US 6373085	20020416	24	Semiconductor memory cell having two epitaxi	257/301	257/302;		Hieda, Katsuhiko et al.	P	P	P	P	P
8	P	P	P	P	US 6135247	20020101	10	Integrated circuit having vertical trench device	438/270	257/E21.65		Tews, Helmut Horst et al.	P	P	P	P	P
9	P	P	P	P	US 6211544	20010403	18	Memory cell layout for reduced interaction bet	257/296	257/300;		Park, Young-Jin et al.	P	P	P	P	P
10	P	P	P	P	US 5656544	19970812	15	Process for forming a polysilicon electrode i	438/386	257/301;		Bergendahl, Albert et al.	P	P	P	P	P
11	P	P	P	P	US 5399516	19950321	15	Method of making shadow RAM cell having a shall	438/589	257/E21.64		Bergendahl, Albert S. et al.	P	P	P	P	P
12	P	P	P	P	US 5196722	19930323	18	Shadow ram cell having a shallow trench eeprom	257/304	257/320;		Bergendahl, Albert S. et al.	P	P	P	P	P
13	P	P	P	P	US 5102817	19920407	16	Vertical DRAM cell and	438/242	257/E27.09		Chatterjee, Pallab et al.	P	P	P	P	P